Remarks

Claims 1-19 are pending in the application.

Claims 14-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 6,069,516 issued to Vargha on May 30, 2000.

Claims 16-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 5,821,825 issued to Kobayashi on October 13, 1998.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vargha in view of United States Patent No. 6,028,496 issued to Ko et al. on February 22, 2000.

Each of the various rejections and objections are overcome by amendments which are made to the specification, drawing, and/or claims, as well as, or in the alternative, by various arguments which are presented.

Rejection Under 35 U.S.C. 112, Second Paragraph

Claims 14-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 14, the Office Action states that "the range" lacks antecedent basis, because it is not understood what the voltage range of a power supply is. The term "range" has been eliminated from the claim and it is now indicated that the voltage is a "beyond voltage" which is defined in the claim to be either greater than the highest or less than the lowest voltage supplied by the power supply.

Regarding claim 16, there is no need to recite how the voltage of line 3 is generated since the purpose of the claims is not to teach the invention, but to define it. Thus, it is sufficient that the claim simply recites that the voltage is generated on the chip. How or where it is generated is immaterial. Thus, this ground of rejection is traversed.

Regarding claims 17 and 18, the Office Action's statements are incorrect. The letter "N" in "NMOS" indeed does stand for negative, and the letter "P" in "PMOS" does indeed stand for positive. This is well known in the art.

Rejection Under 35 U.S.C. 102(b)

Claims 14-19 are rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 6,069,516 issued to Vargha on May 30, 2000.

The Office Action states that FIG. 2 of Kobayshi discloses an active inductor (22) biased by the voltage divider (R3, R4) which provides a reference voltage between the voltage Vee and ground or beyond the Vee.

These grounds of rejection are respectfully avoided for the following reasons.

Vargha

Vargha fails to teach using a MOSFET as an active inductor as recited in applicant's claims. Instead, Vargha teaches using the MOSFET as a switch.

More specifically, in Vargha, the MOSFET is operated in one of two modes: either a) the MOSFET is completely off, which is in the operating region known as cutoff, or b) the MOSFET is completely on, which is in the operating region know as the so-called "triode", "linear" or "ohmic" region, which are all alternative names for the same region given in different text books. By contrast, applicant operates the MOSFET to make it look like an inductor. To do so, the MOSFET is operated in the so-called "active", "pinchoff" or "saturation" region, which are all alternative names given in different text books for the region in which the drain-to-source voltage is greater than the gate-to-source voltage minus the threshold voltage. Note that the region in which applicant's invention operates the MOSFET is different than either of the regions employed by Vargha for the switch.

Thus, the teaching of a switch in Vargha does not anticipate applicant's claim of an active inductor, and so Vargha does not teach or suggest applicant's independent claims 14, and 16, so that applicant's claims 14 and 16 are allowable over Vargha.

Since claims 15 and 17-19, respectively, depend on and include all the limitations of claim 14 and claim 16, respectively, which are allowable over Vargha, claims 15 and 17-19 are also allowable over Vargha.

Kobayashi

In Kobayashi, Vee and ground are the voltages supplied by the power supply of Kobayashi, and so, as will be readily recognized by those of ordinary skill in the art, Vee and ground form the range of the DC supply voltage for the Kobayashi circuit. As previously stated, as is well known, according to basic electrical engineering principles, the voltage at the middle of a voltage divider will be a value that is between the values at the ends of the divider. Thus, since the voltage divider cited by the Office Action is connected between Vee and ground, the bias voltage produced by the Kobayashi voltage divider of R3 and R4 must be between Vee and ground, i.e., between the highest and lowest voltage supplied by the power supply. Consequently, the Kobayashi arrangement does not operate as does applicants' independent claim 16, in that the active inductor of Kobayashi is **not** biased using a voltage outside the range of voltage supplied by a power supply for operating the integrated circuit. Instead, the Kobayashi arrangement operates to bias its active inductor using a voltage generated on said integrated circuit that is **within** the range of the voltage supplied by a power supply for operating the integrated circuit.

Therefore, Kobayashi does not teach or suggest applicant's independent claim 16, and applicant's claim 16 is allowable over Kobayashi.

Since claims 17 and 19 depend on and include all the limitations of claim 18, which is allowable over Kobayashi, claims 17 and 19 are also allowable over Kobayashi

Rejection Under 35 U.S.C. 103(a)

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vargha in view of United States Patent No. 6,028,496 issued to Ko et al. on February 22, 2000.

The Office Action states that Vargha discloses all of the limitations of the claimed invention but does not disclose a resistor. However, continues the Office Action, Ko et al., teach a circuit comprising resistors (R2-R8) for reducing current to the transistors in order to protect these transistors. Therefore, concludes the Office Action, it would have been obvious to a person of ordinary skill in the art to employ the resistor as taught by Ko et al. in the circuit of Vargha for purpose of protecting the transistor.

Applicant respectfully traverses this ground of rejection for the following reasons.

First, as noted above, Vargha teaches operating a MOSFET as a switch, not as an active inductor. There is no suggestion in Vargha that any teaching therein is applicable to an active inductor. Furthermore, as shown above, the arrangements taught in Vargha operate the MOSFET only in operating regions that are not employed when a MOSFET is operated as an active inductor.

Second, notwithstanding the Office Action's statements to the contrary, the resistors R2-R8 are not for "protecting" the MOSFETs as stated by the Office Action. Instead, they are required to bias the MOSFETs so as to achieve operation of the circuit as an active inductor. (See Ko et al., column 4, lines 2-12.) More specifically, the resistor is an essential part of the active-inductor circuit in that a mathematical analysis shows that this resistor interacts with the gate-source capacitance and the transconductance of the MOSFET to produce an inductor. In fact, the value of the active inductor, i.e., the inductance of the active inductor, is controlled by the value of the gate resistor

Thus, there is no motivation to include resistors R2-R8 in the circuit of Vargha. Furthermore, the teaching of Ko et al. is actually away from doing so, since to do so

would prevent the arrangement of Vargha from operating in its prescribed manner as a switch.

Since there is no teaching, suggestion, or motivation to combine Vargha with Ko et al., applicants claims 1-13 are allowable over Vargha and Ko et al. applicant's claims are allowable over the purported combination.

Conclusion

It is respectfully submitted that the Office Action's rejections have been overcome and that this application is now in condition for allowance. Reconsideration and allowance are, therefore, respectfully solicited.

If, however, the Examiner still believes that there are unresolved issues, he is invited to call applicant's attorney so that arrangements may be made to discuss and resolve any such issues.

In the event that an extension of time is required for this amendment to be considered timely, and a petition therefor does not otherwise accompany this amendment, any necessary extension of time is hereby petitioned for, and the Commissioner is authorized to charge the appropriate cost of such petition to the **Lucent Technologies Deposit Account No. 12-2325**.

Respectfully,

Eduard Sackinger

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Date: 2-14-02

MARKED-UP VERSIONS OF THE AMENDED CLAIMS

IN THE CLAIMS

Unchanged claim 1

1. An active inductor for use on an integrated circuit having a power supply voltage supplied from a first power supply terminal, comprising:

an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to said power supply voltage and said source terminal being one of the terminals of said active inductor; and

a resistor having a first terminal coupled to said gate terminal and a second terminal coupled to a voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Unchanged claim 2

2. The invention as defined in claim 1 wherein the other one of the terminals of said active inductor is said first power supply terminal.

Unchanged claim 3

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

Unchanged claim 4

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 5

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 6

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

Unchanged claim 7

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

Unchanged claim 8

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

Unchanged claim 9

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

Unchanged claim 10

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

Unchanged claim 11

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

Unchanged claim 12

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Unchanged claim 13

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

Replacement claim 14

14. (Amended) An active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a ~~high~~ beyond voltage generator which generates a beyond voltage that is either ~~voltage outside the range of voltages~~ greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said ~~high~~ beyond voltage generator so as to bias said MOS transistor with said beyond voltage ~~outside the range of voltages being supplied to said integrated circuit by a power supply~~ and so that said MOS transistor operates as said active inductor.

Replacement claim 15

15. (Amended) The invention as defined in claim 14 wherein said ~~high~~ beyond voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is ~~outside the range of voltages~~ either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is outside the range of volta~~-outside the range of voltages~~ greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said ~~fs~~ beyond voltage generator.

Replacement claim 16

16. (Amended) An active inductor on an integrated circuit, said active inductor comprising a metal oxide semiconductor (MOS) transistor that operates as said active inductor and being characterized in that said active inductor is biased using a voltage generated on said integrated circuit that is ~~beyond~~ outside the range of the voltage supplied by a power supply for operating said integrated circuit.

Unchanged claim 17

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

Unchanged claim 18

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

Unchanged claim 19

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.